Texas Instruments Keynote

Title: Challenges and Trade-offs in Integrated Transceiver Architectures for High Performance 5G Wireless Base Stations

Abstract:

5G communication technology offers high data rates by increasing the spectral efficiency, using wider bandwidth and multiple frequency bands. 5G base stations employ beamforming and massive MIMO techniques with large number of antennas like 32 transmit and 32 receive (32T32R) or 64T64R systems. The base stations require integrated transceiver System on Chip (SoC) solutions with multiple transmit, receive and feedback channels as basic building modules of the system. Some of the key requirements of integrated transceiver SoCs for 5G base stations are high performance, low power consumption and small form factor. The architecture chosen for the integrated transceiver has direct impact on various system aspects like bandwidth support, complexity of the signal processing algorithms to calibrate transmit (TX) and receive (RX) RF/Analog impairments and power consumption. Zero-IF and RF Sampling architectures are the possible choices for high performance integrated transceivers. In this talk, we discuss the system level challenges in signal processing algorithms for TX and RX RF/Analog impairment estimation like IQ mismatch (IQMM) estimation, LO leakage estimation and TX chain Digital Pre-distortion (DPD) in Zero-IF transceivers. We then present the RF Sampling architecture where the RF/Analog signal is directly sampled by a high-speed RX ADC to convert to a digital signal or vice-versa by a TX DAC in transmit chain. We show that RF sampling architecture avoids the RF/Analog impairments of IQ mismatch and LO leakage to reduce the system design complexity and can also lower the system complexity of TX DPD estimation. RF sampling architecture enables high performance wide bandwidth transceivers with multi-band transmission/reception capability and is well suited to meet the 5G base station demands.

About the speaker:

Sarma Gunturi is a Principal Systems Engineer and Distinguished Member of Technical Staff with the Analog Signal Chain department at Texas Instruments, Bangalore. He received his B.Tech. degree in Electrical Engineering from IIT, Bombay, in 2000, and M.S. in Electrical Engineering from University of California Los Angeles in 2002. After his M.S. he joined Texas Instruments (TI) in 2002 and, at TI, his work has been in the field of Signal Chain Architectures, RF systems analysis, Signal Processing Algorithms and Communication Systems for 4G/5G transceivers, WLAN and Heart Rate Monitoring.

Sarma has developed architectures and signal processing algorithms for various highly integrated, high performance and low power consumption system-on-chip solutions for mobile WLAN and wireless base stations. He holds over 30 patents with the US Patent Office and is the recipient of the INAE Young Engineer Award in 2014.